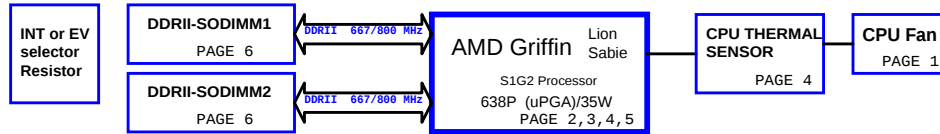


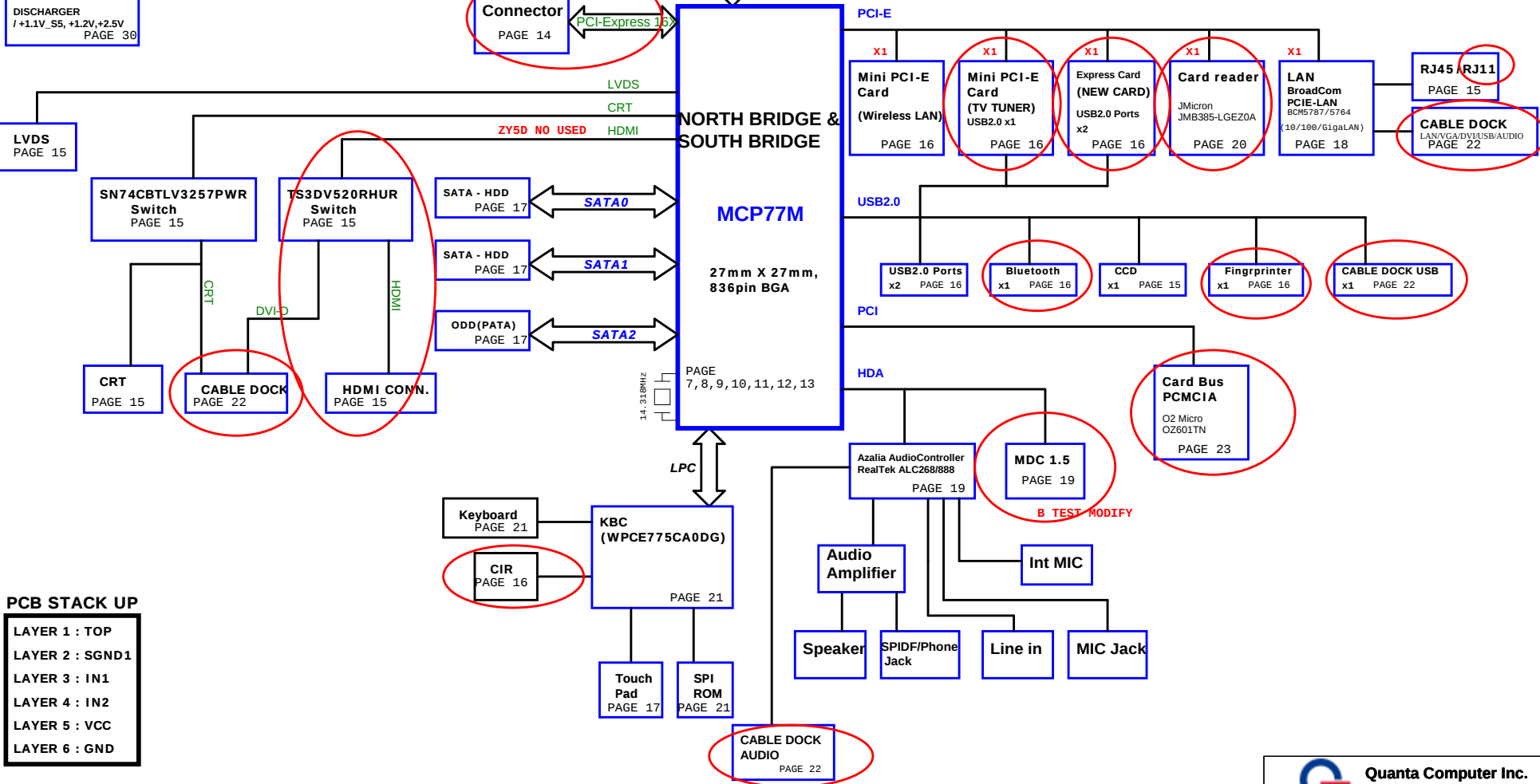
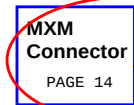
ZY5/ZY5D SYSTEM BLOCK DIAGRAM



CPU CORE ISL6265A	PAGE 26
NB CORE +1.1V	PAGE 27
NB RUN +1.1V	PAGE 28
DDR II SDDR_VTERM 1.8VSUS(TPS51116REG)	PAGE 29
SYSTEM POWER ISL6237	PAGE 25
SYSTEM CHARGER (ISL6251A)	PAGE 24
DISCHARGER / +1.1V_S5, +1.2V, +2.5V	PAGE 30



ZY5D NO USED





PROCESSOR HYPERTRANSPORT INTERFACE

VLDLT_Ax AND VLDLT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

REV:B Modify

VLDLT_RUN

U25A

HT LINK

VLDLT_A0

VLDLT_A1

VLDLT_A2

VLDLT_A3

VLDLT_B0

VLDLT_B1

VLDLT_B2

VLDLT_B3

AE2

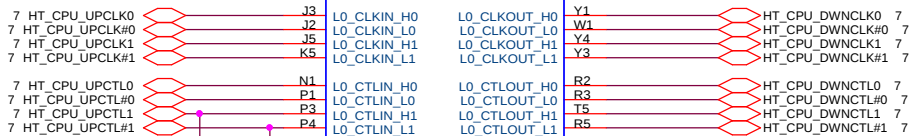
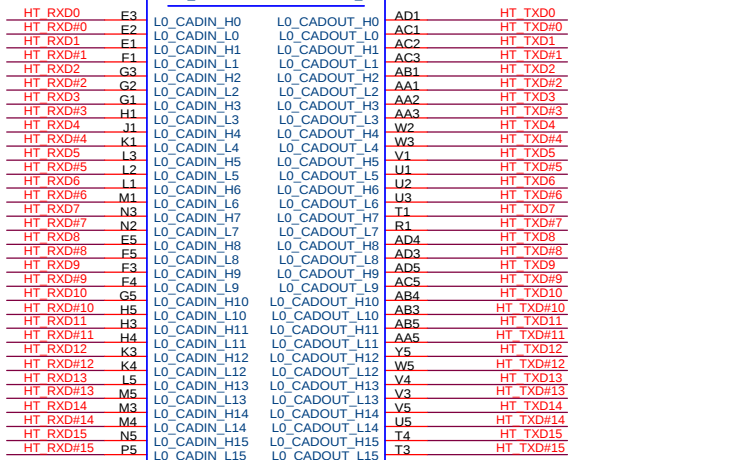
AE3

AE4

AE5

C496

4.7u/6.3V_6



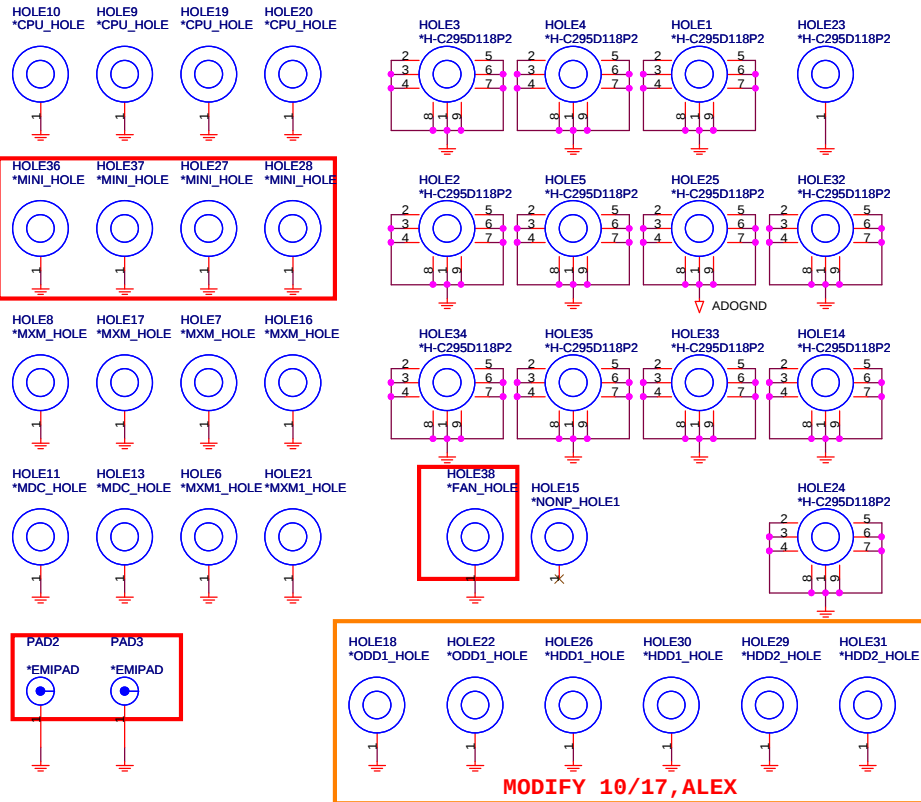
NO STUB for HT3

R189 *51/F_4

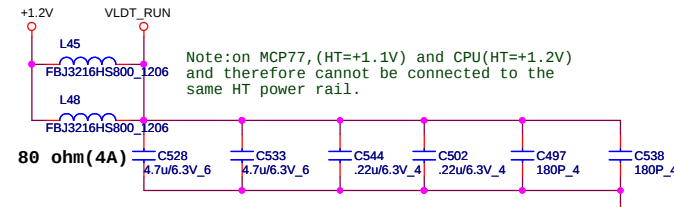
R187 *51/F_4

VLDLT_RUN

Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN



MODIFY 10/17, ALEX



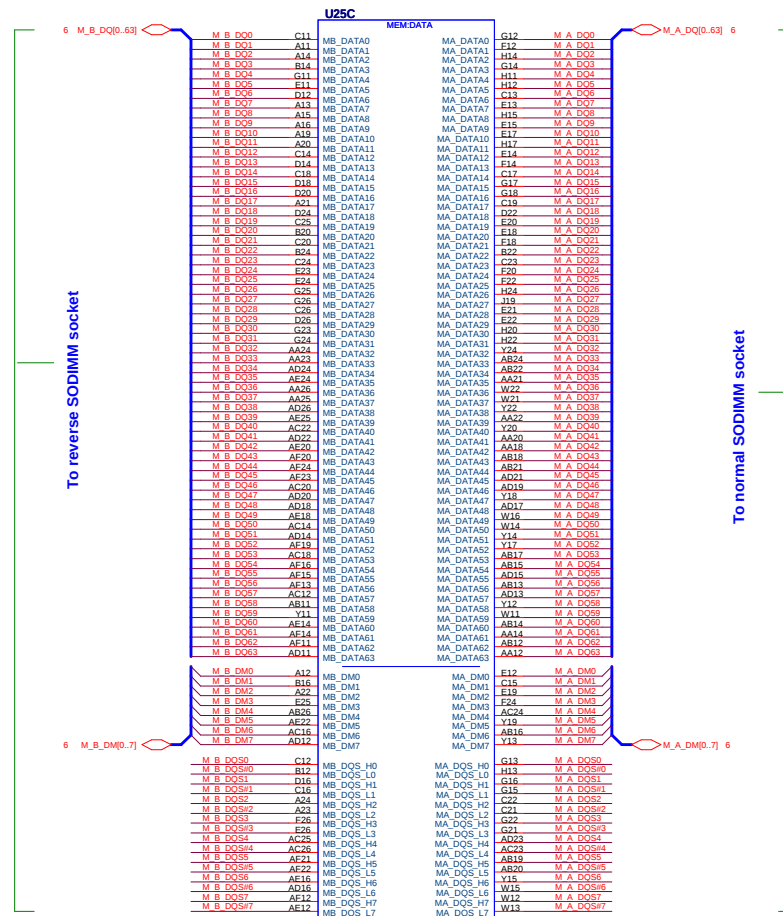
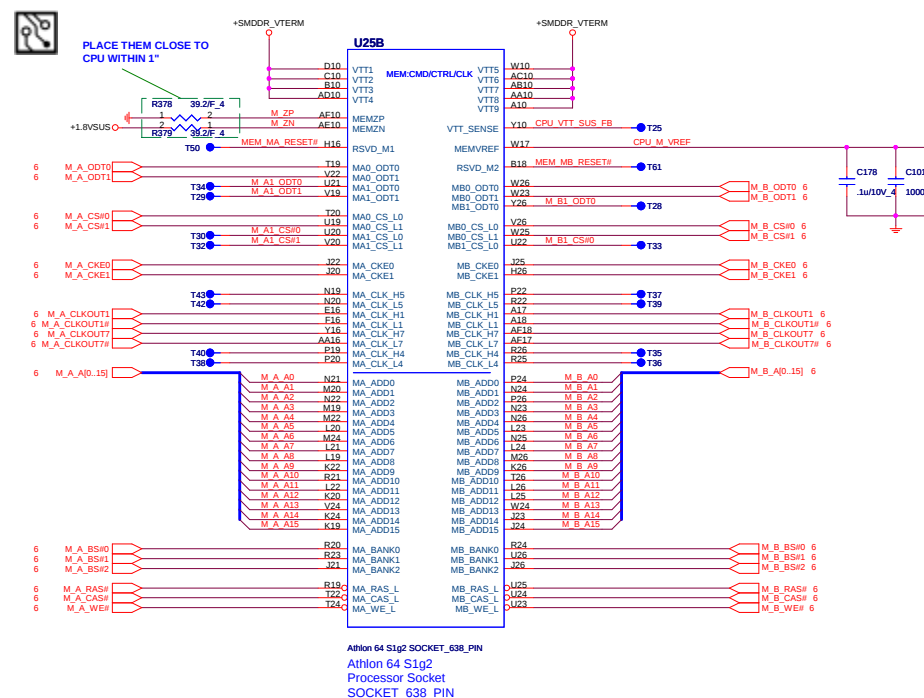
LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDLT0 POWER PINS

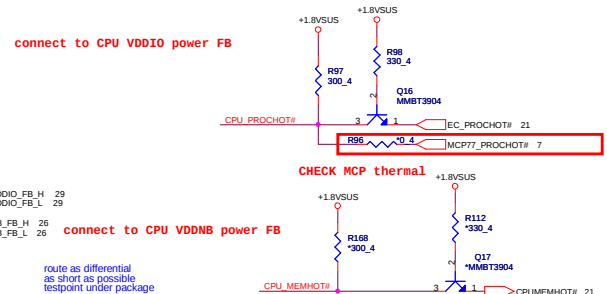
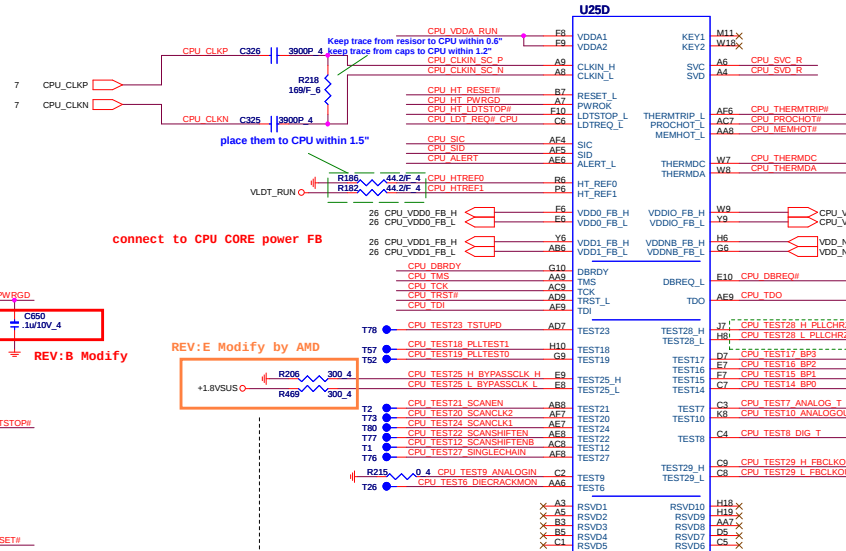
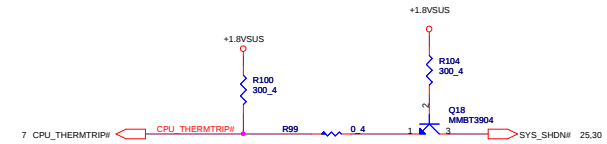
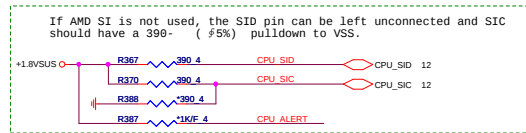
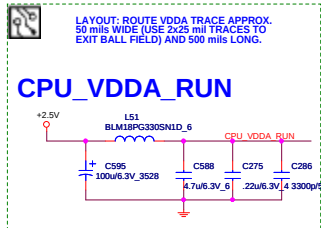


Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	AMD Griffin HT I/F	3B
Date:	Wednesday, May 21, 2008	Sheet 2 of 35

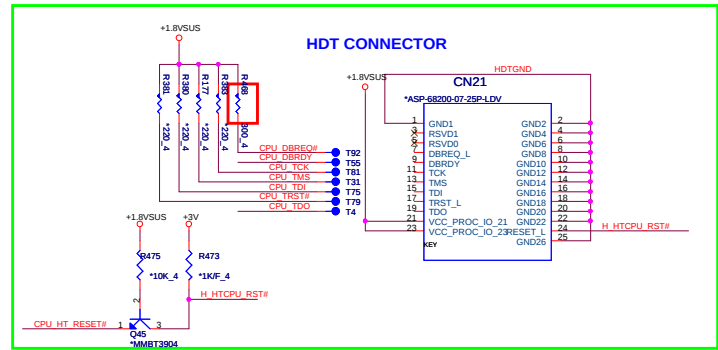
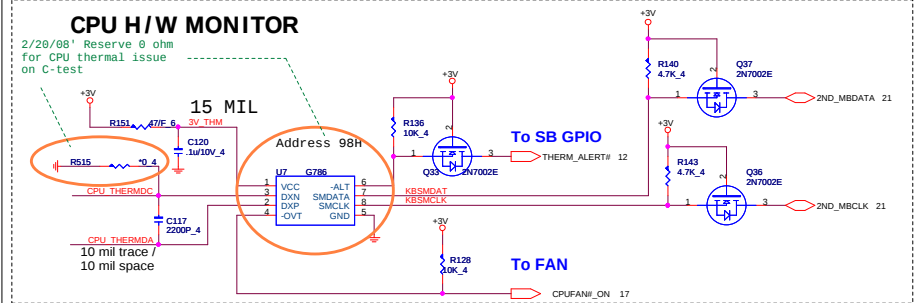
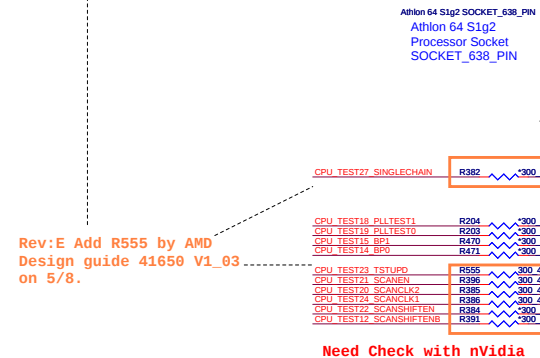
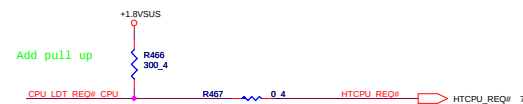


ATHLON Control and Debug

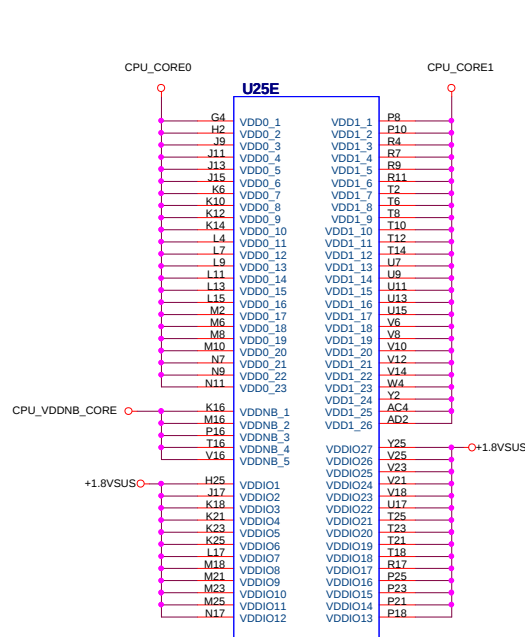


VFIX MODE

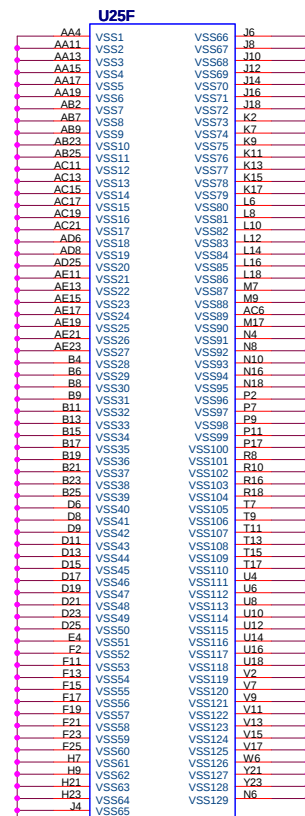
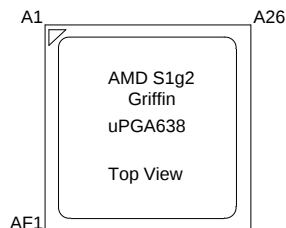
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



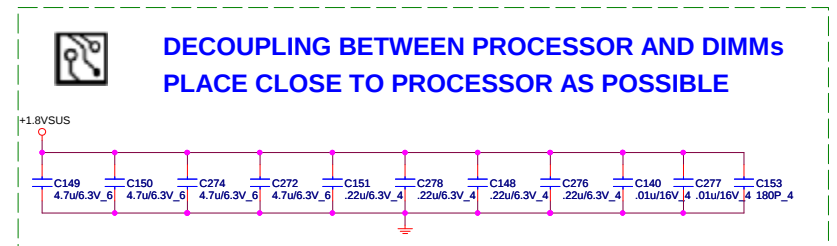
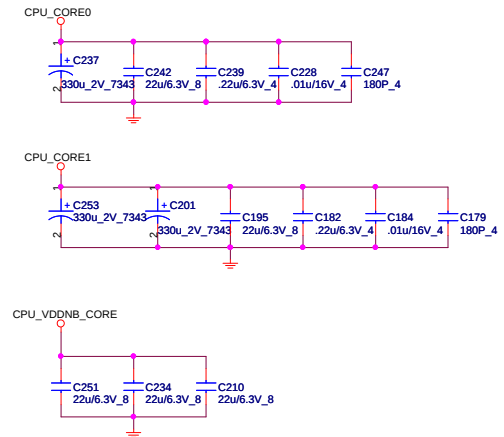
PROCESSOR POWER AND GROUND



Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN



Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN

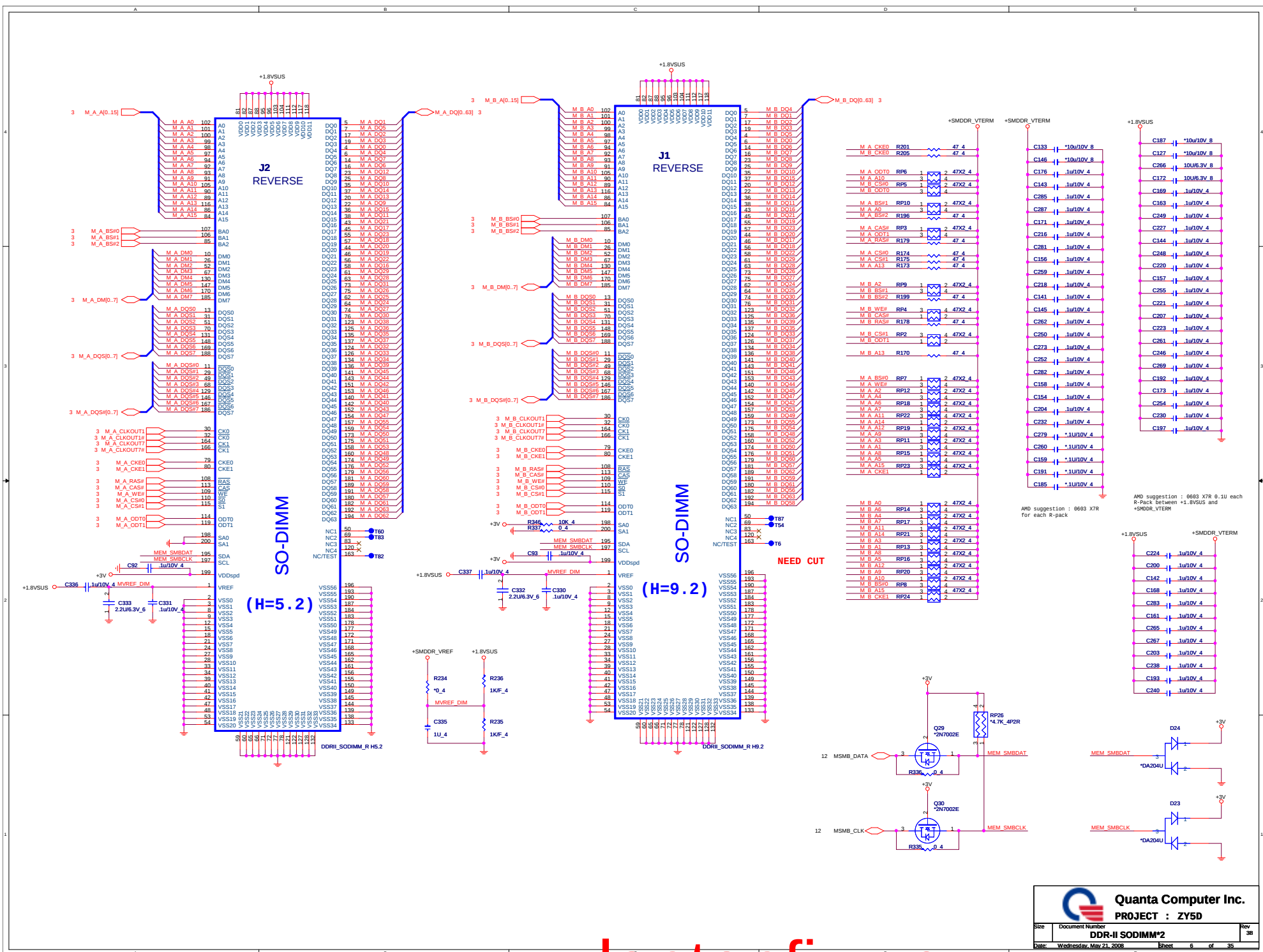


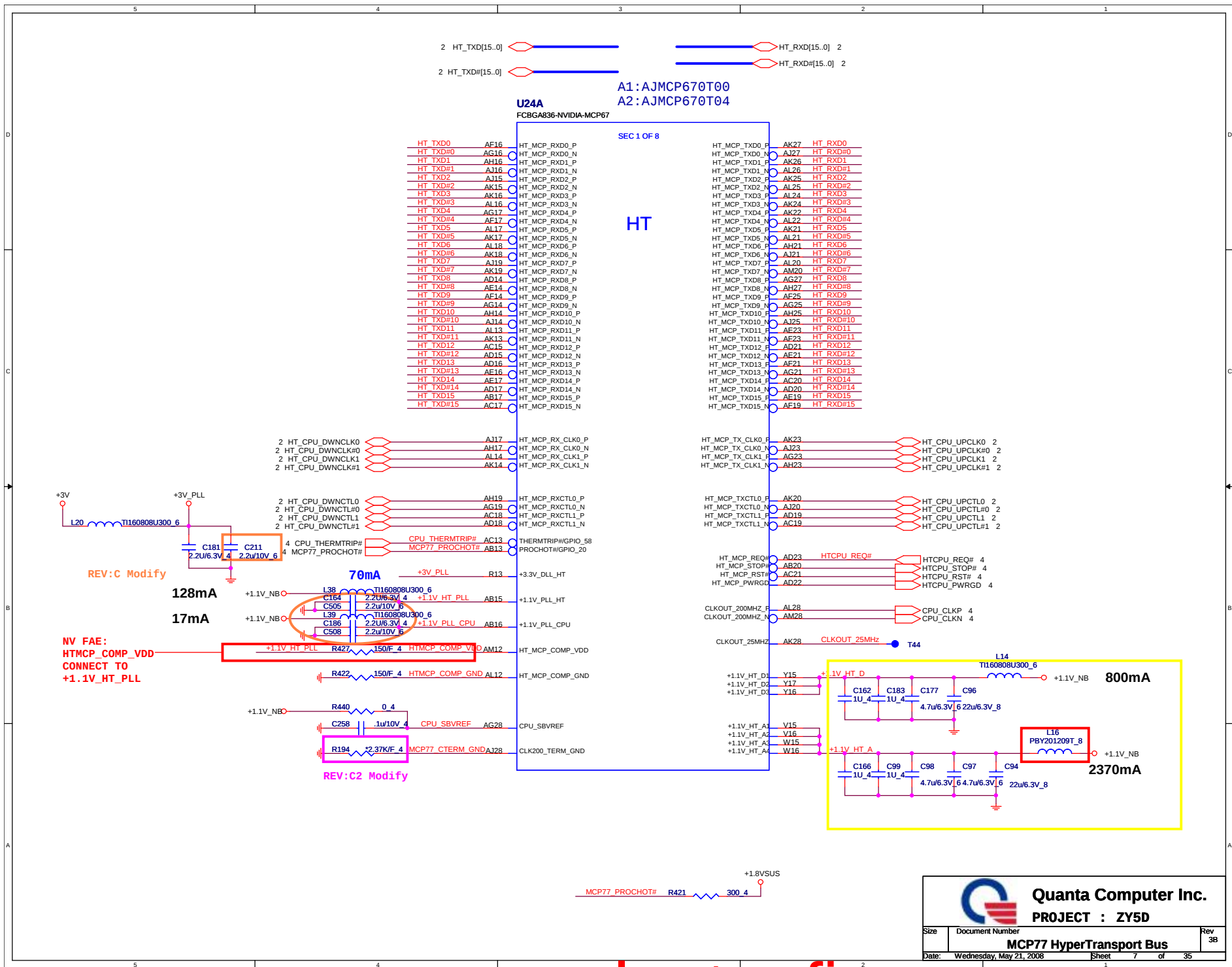
**DECOUPLING BETWEEN PROCESSOR AND DIMMS
PLACE CLOSE TO PROCESSOR AS POSSIBLE**



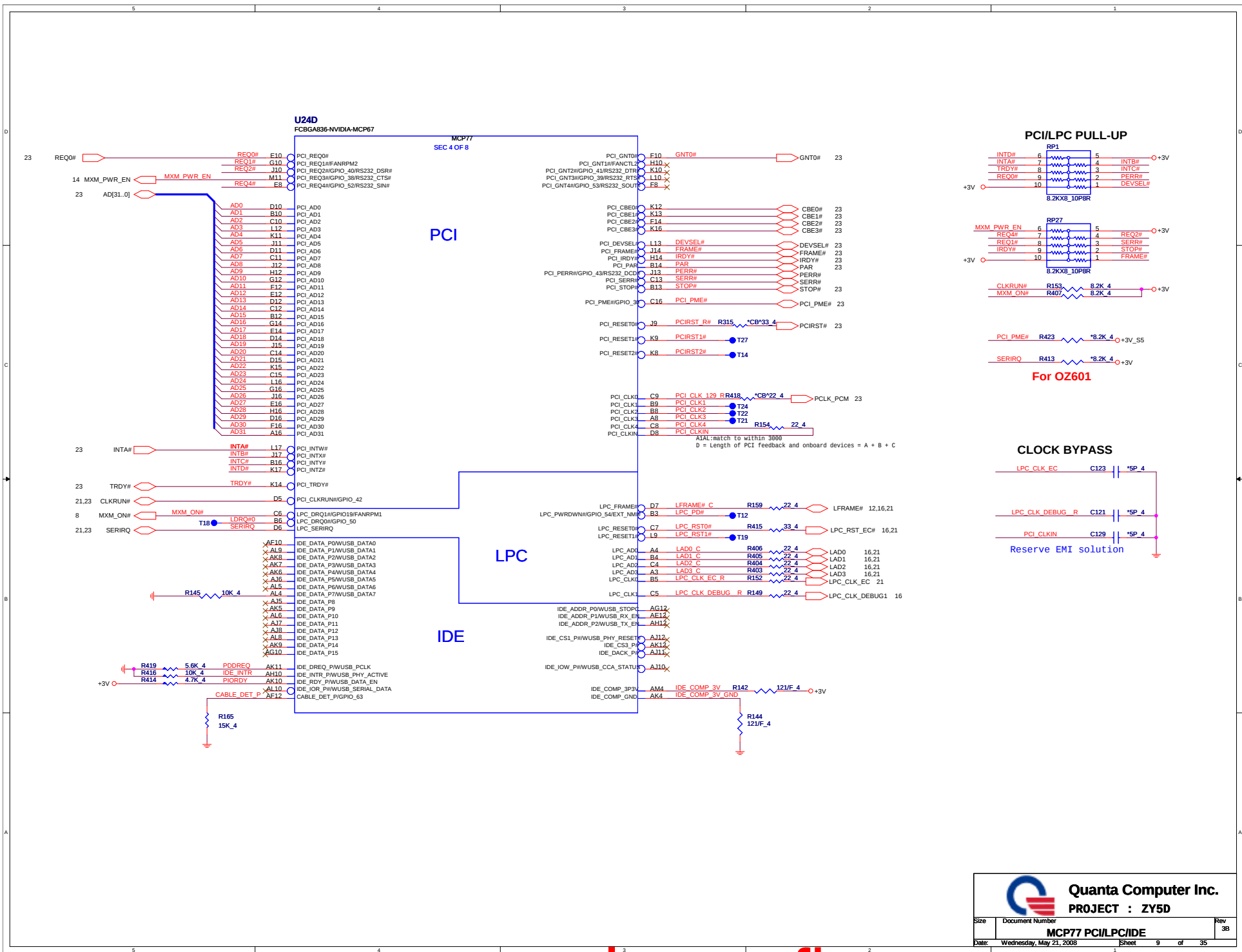
Quanta Computer Inc.
PROJECT : ZY5D

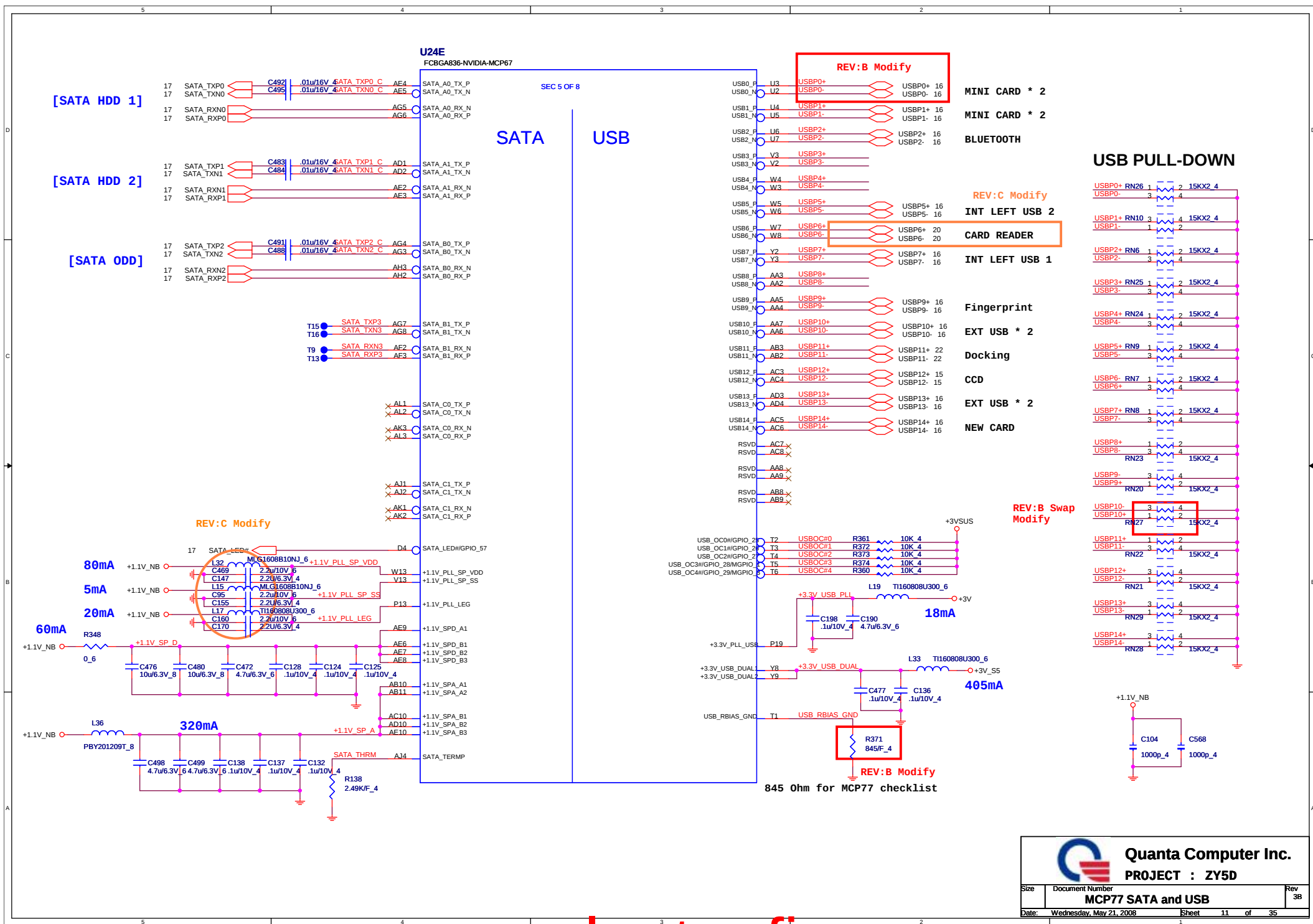
Size	Document Number	Rev
	AMD Griffin PWR & GND	3B
Date:	Wednesday, May 21, 2008	Sheet 5 of 35



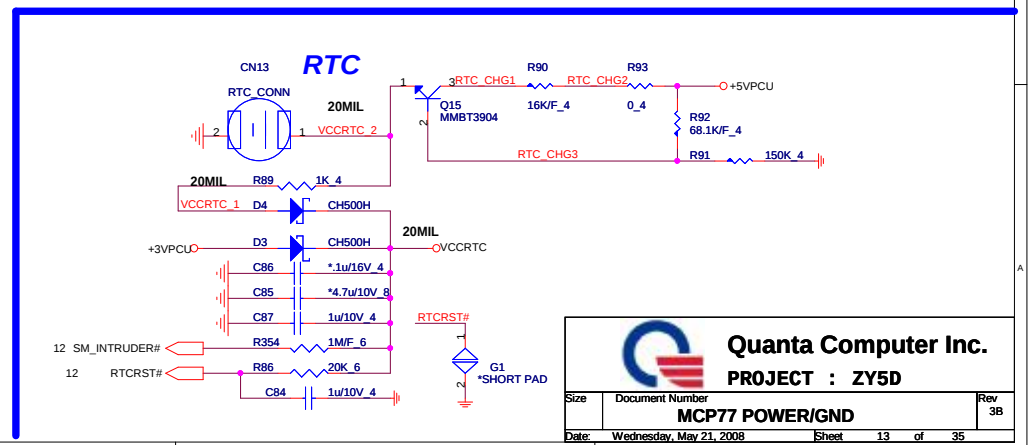
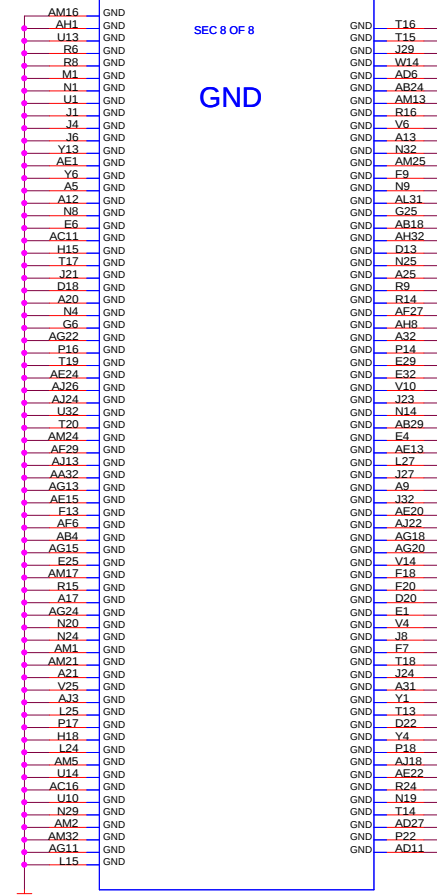
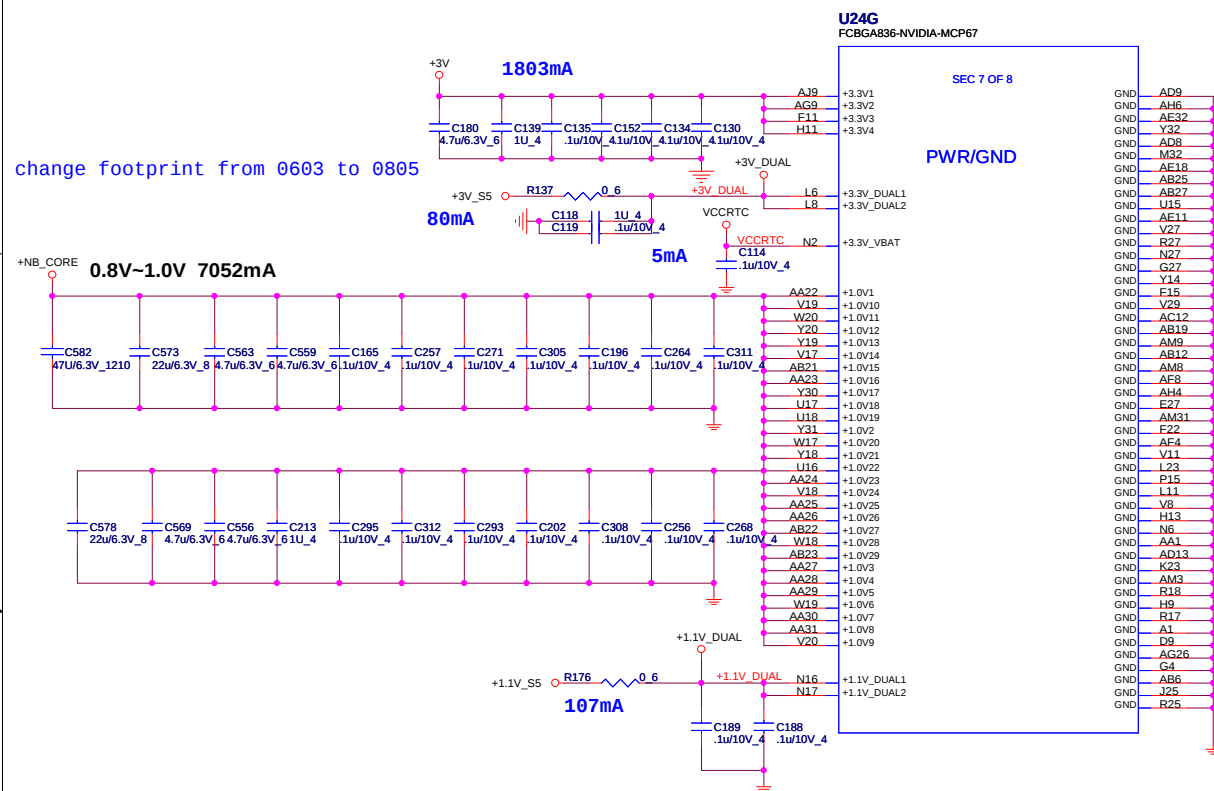




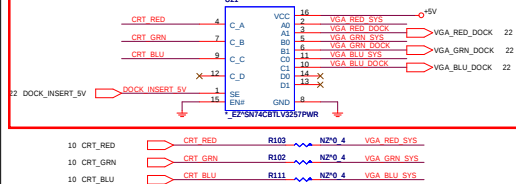
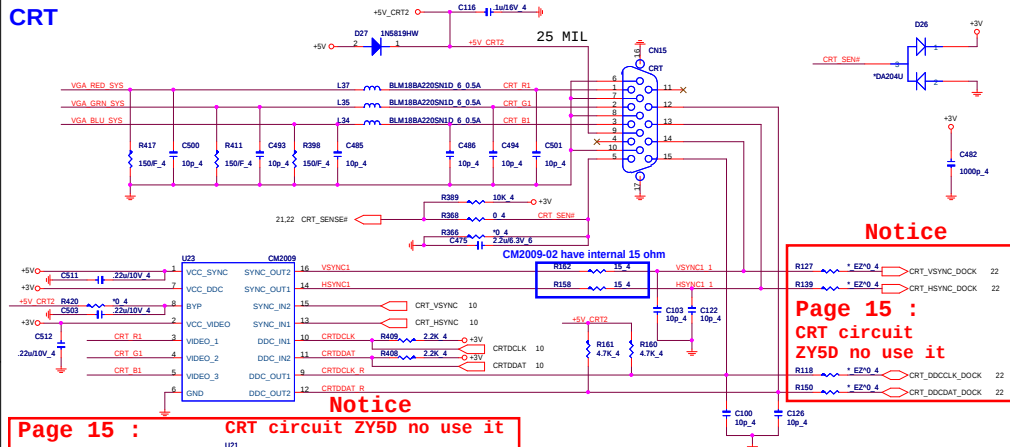




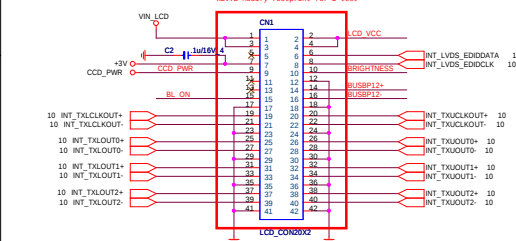
MCP77 POWER PLANE/GND & BYPASS



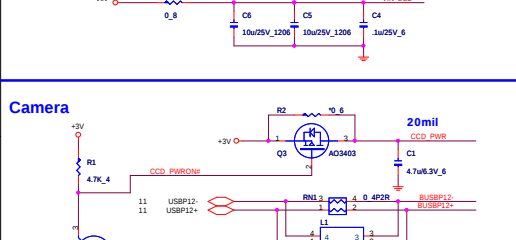
CRT



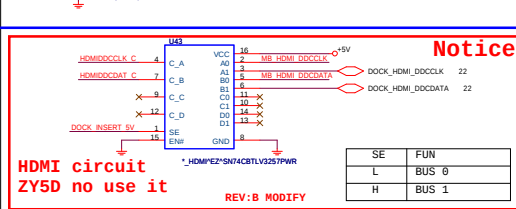
LVDS



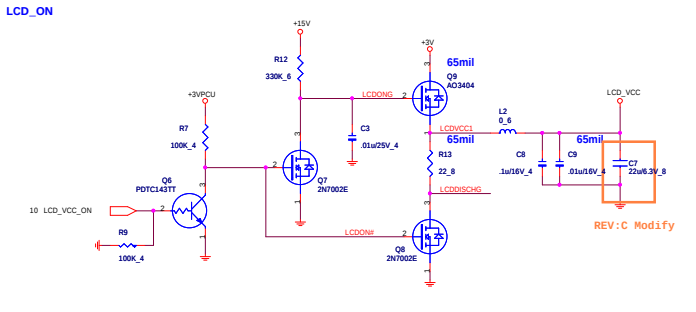
Camera



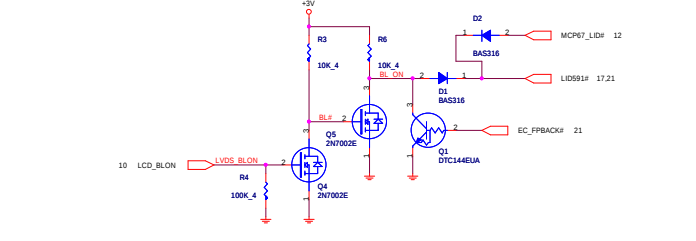
HDMI



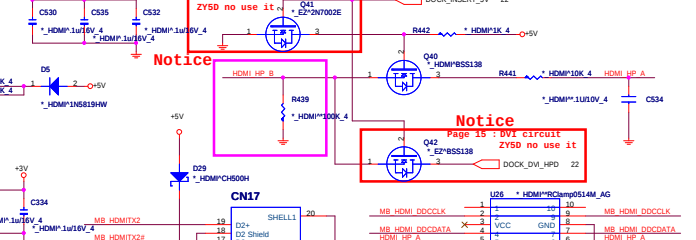
LCD_ON



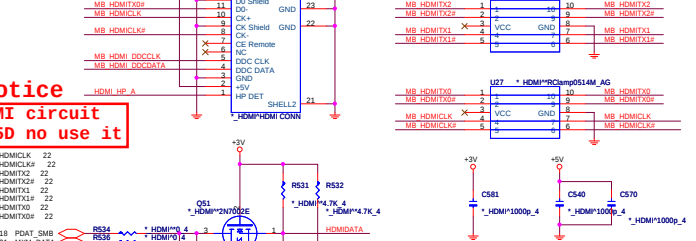
Backlight Control



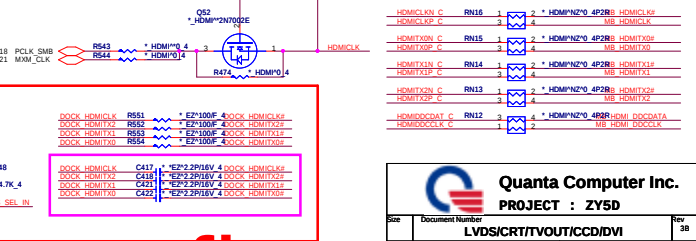
HDMI



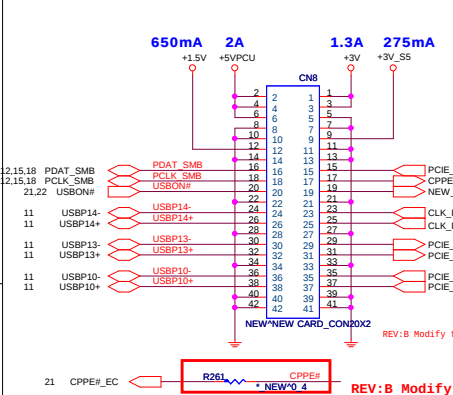
HDMI



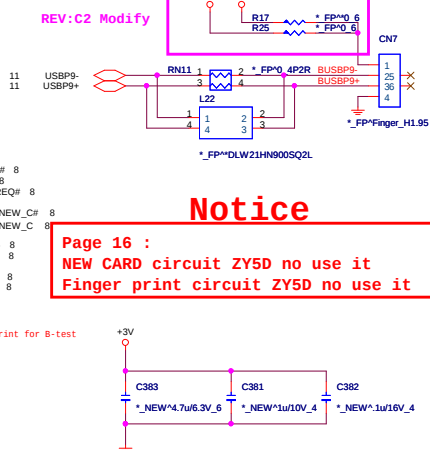
HDMI



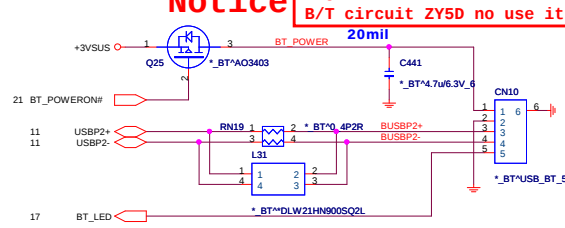
To NEW-CARD & EXT. USB



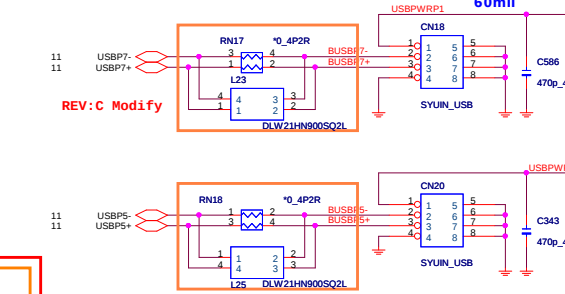
Fingerprint



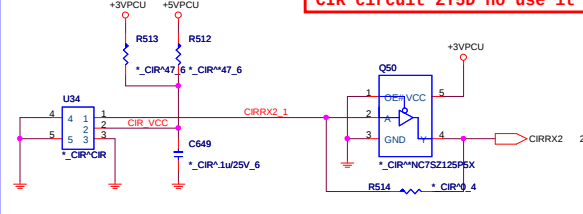
Bluetooth



INT. USB

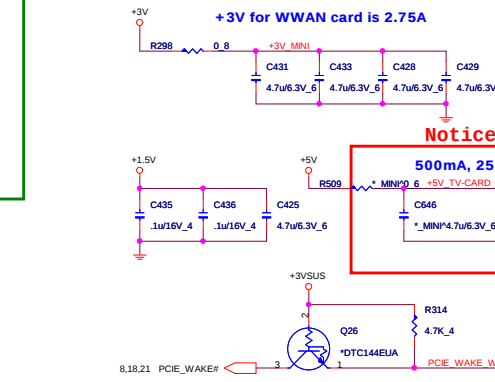
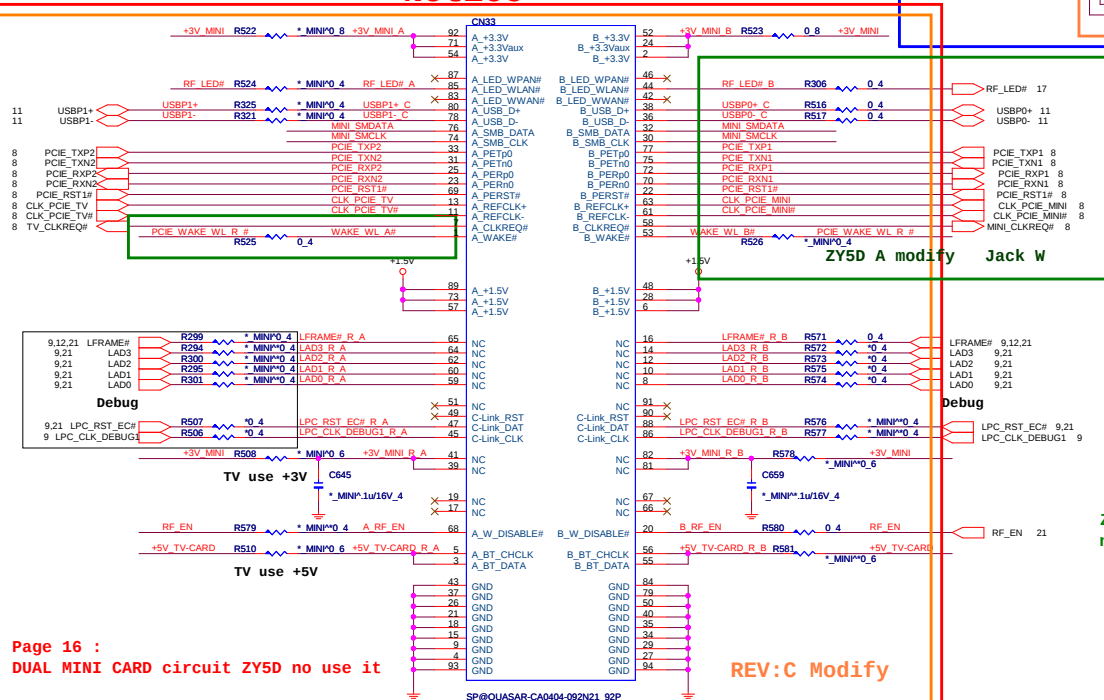


CIR

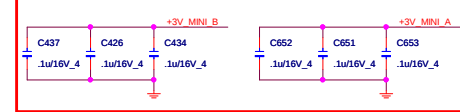


MINI-CARD

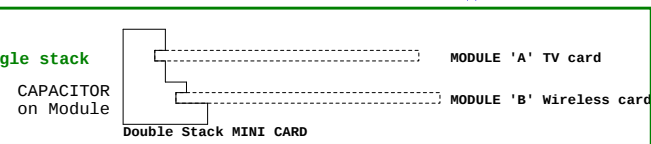
Notice



REV:B Modify



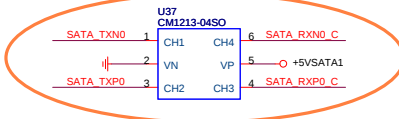
ZY5D B test has modified to single stack
no TV card, only Wireless card



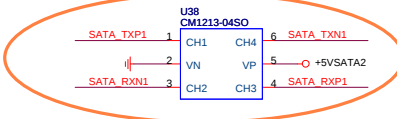
Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	NEW&MINI&TV CARD/USB/BT/CIR	38
Date	Thursday, July 24, 2008	Sheet 16 of 35

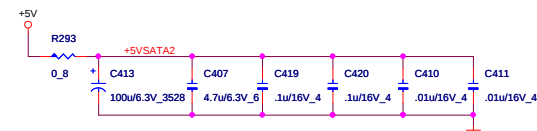
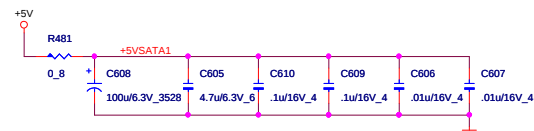
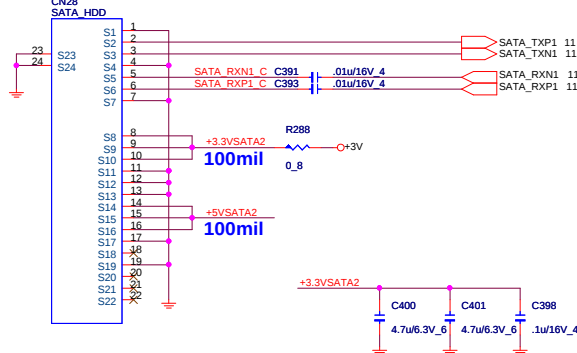
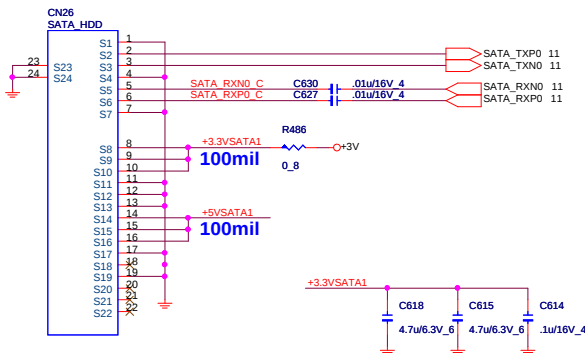
SATA1



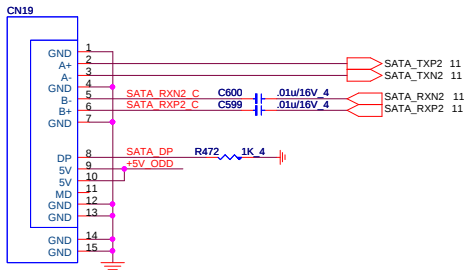
SATA2



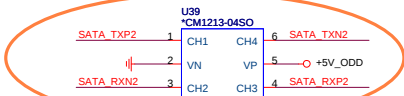
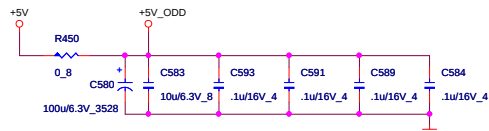
REV:E add ESD



ODD (SATA)

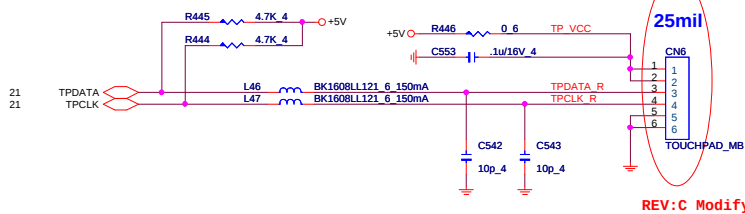


C16654-122A4-1_Serial_ATA



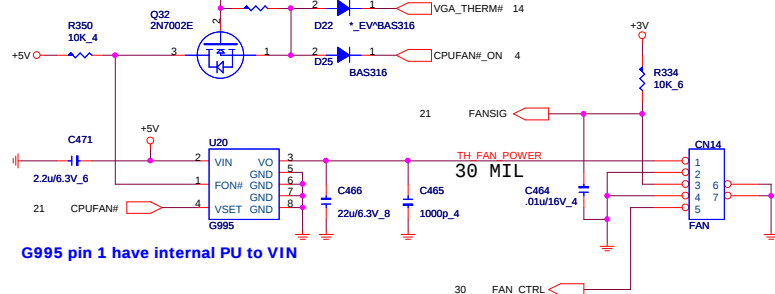
REV:E add ESD

TP CONN



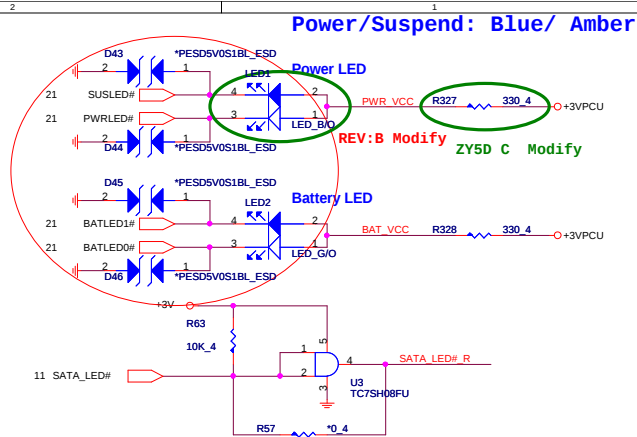
REV:C Modify

FAN



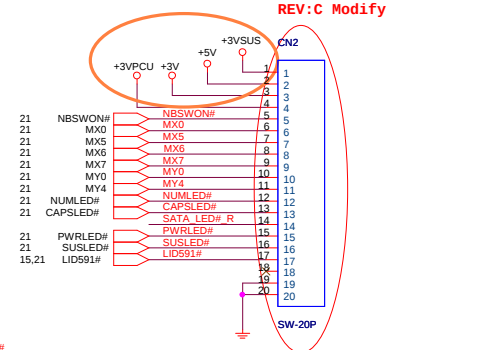
G995 pin 1 have internal PU to VIN

LED



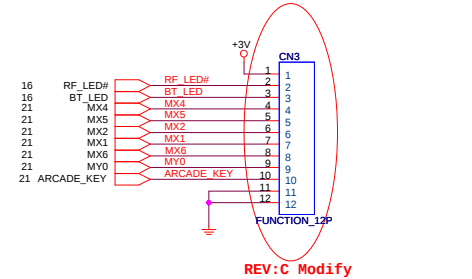
REV:C Modify

To Power/B



REV:B Modify

To Switch/B



REV:C Modify



Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN	3B
Date:	Friday, July 25, 2008	Sheet 17 of 35

[illegible]

EEPROM Strapping

	SO	SI	CS#	SCLK
24C64	1	1	0	1
AT45D08B11B	1	0	1	1

[illegible]

Transformer

Source 1: DELTA

Source 2: Bothand

LFE9249

GST5009

DB0ZR1LAN11

DBKN1NLAN03

Source 1: DELTA

Source 2: Bothand

LFE9249

GST5009

DB0ZR1LAN11

DBKN1NLAN03

REV:B Modify

1500P/2KV 1808

REV:C Modify

REV:B Modify

3V_LAN_SS

R21

R20

LAN_LINKED# SYS 10

LAN_VCC4

GREEN_N

GREEN_P

CN11

X-TXN 9

X-TXP 6

X-TXIN 6

X-TXEN 5

X-RXP 4

X-RXP 3

X-RXIN 3

X-RXP 2

X-RXP 2

TXI-

TXI+

RX1-

RX1+

RX2-

RX2+

RX2-

RX2+

GND2

14

GND1

13

3V_LAN_SS

R14

LAN_ACTLED# SYS 12

LAN_VCC4

YELLOW_N

YELLOW_P

FOXCONN_RJ45

EMI

LAN_VCC3

C25

1u/16V 4

LAN_VCC4

C14

1u/16V 4

LAN_LINKED# SYS C21

1u/16V 4

LAN_ACTLED# SYS C11

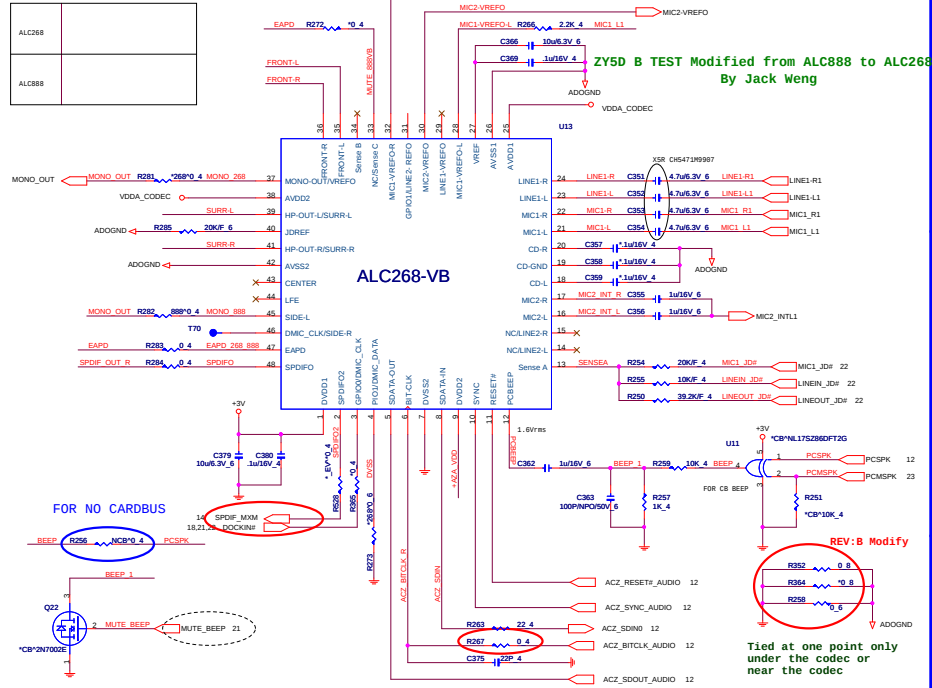
1u/16V 4

ZY5D C TEST Modified footprint from 0402 to 0805 to solve Lan burnt issue on Acer project

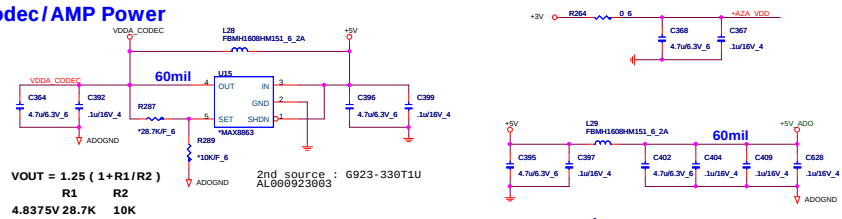
By Jack Wang

ZY5D C TEST Modified footprint from 0402 to 0805
to solve Lan burnt issue on Acer project
By Jack Weng

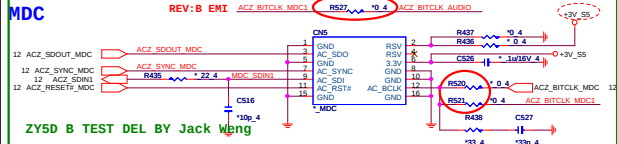
CODEC



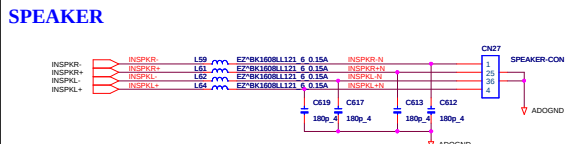
Codec/AMP Power



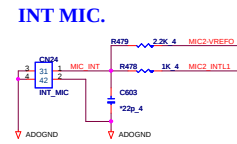
MDC



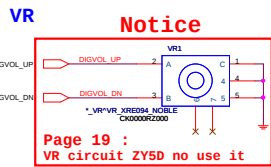
SPEAKER



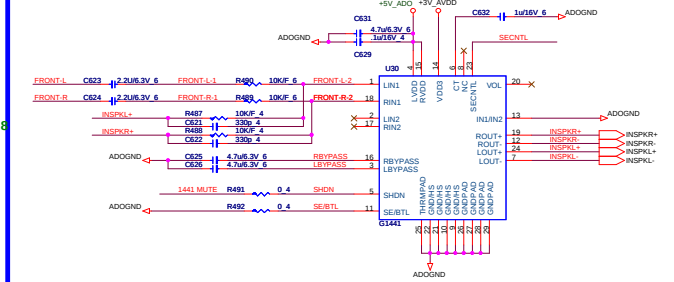
INT MIC.



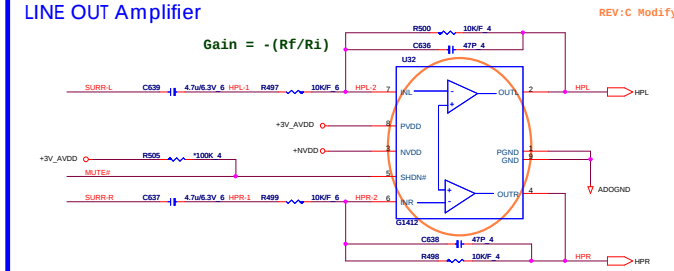
VR



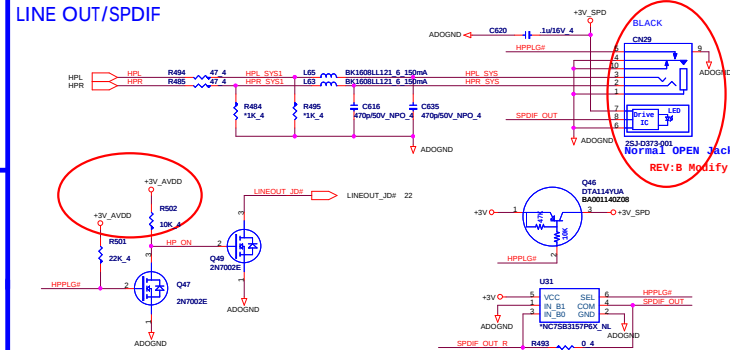
Speaker Amplifier



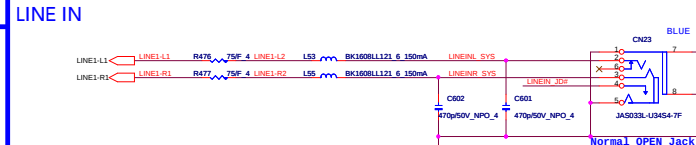
LINE OUT Amplifier



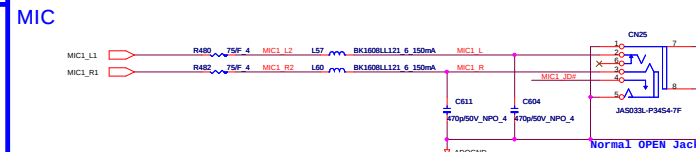
LINE OUT/SPDIF



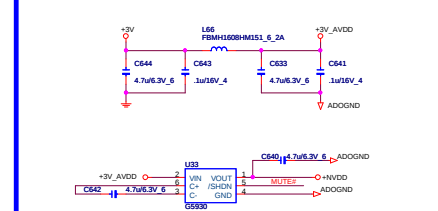
LINE IN



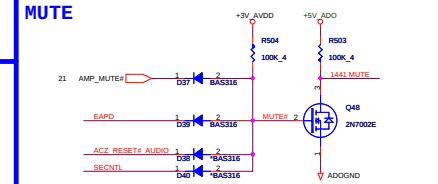
MIC



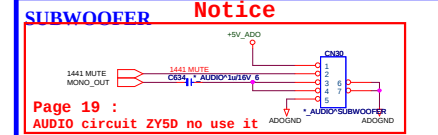
Amplifier POWER



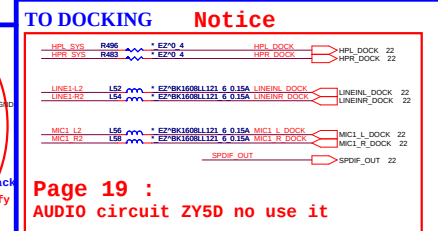
MUTE



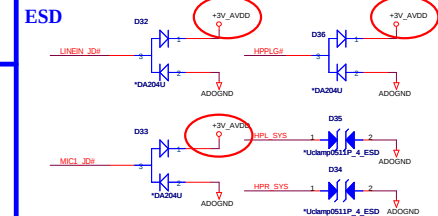
SUBWOOFER



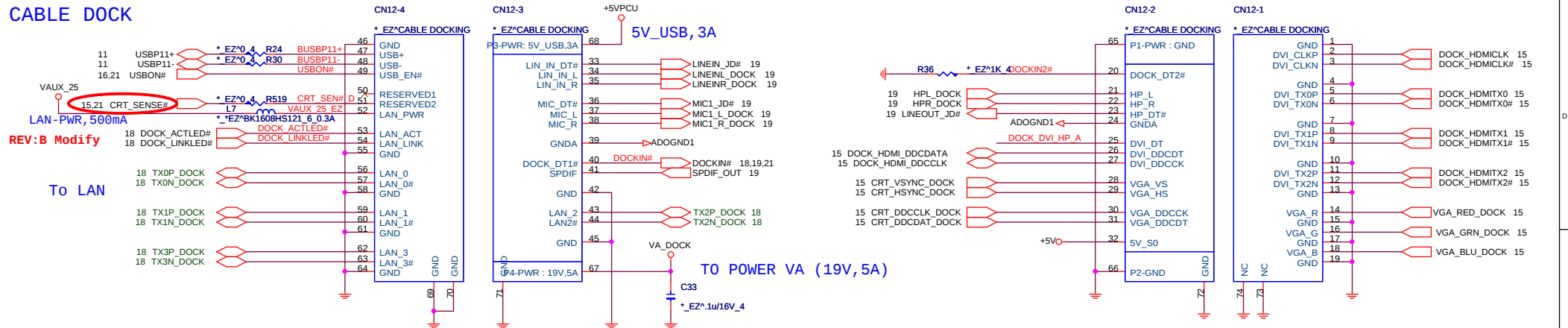
TO DOCKING



ESD



CABLE DOCK



NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

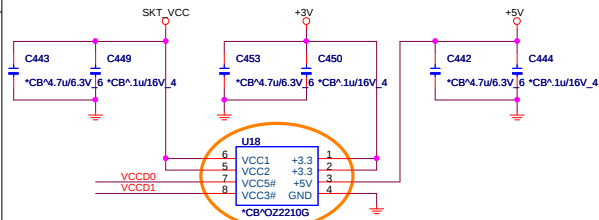
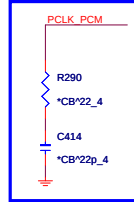
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

ID Select : AD20
 Interrupt Pin : INTA#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#

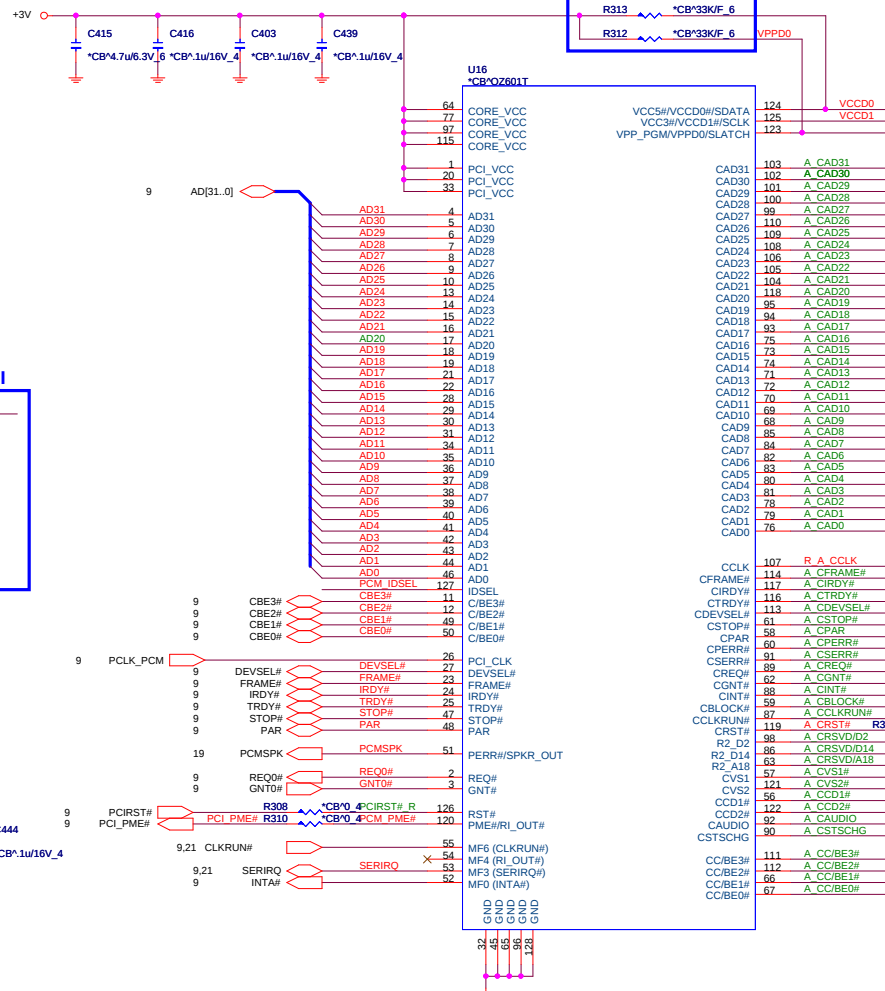
For EMU



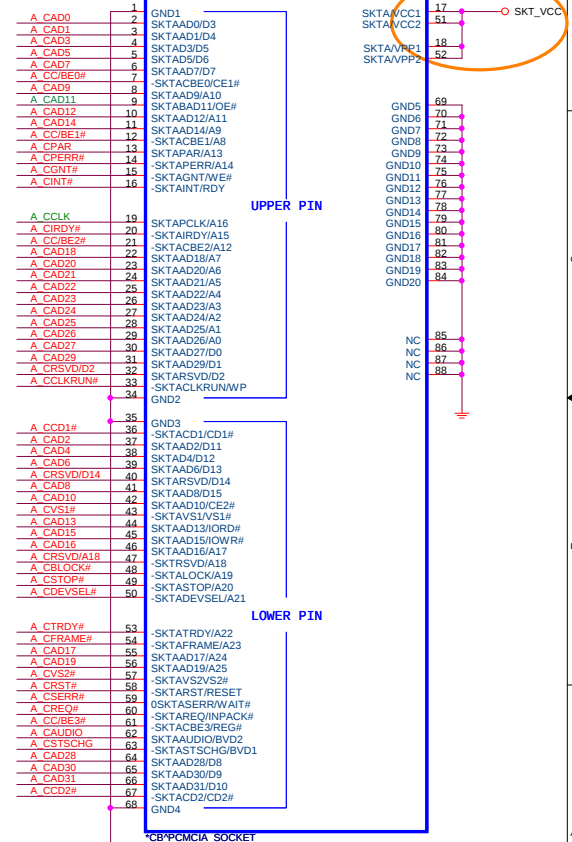
Check Footprint & P/N

22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



PCMCIA SOCKET

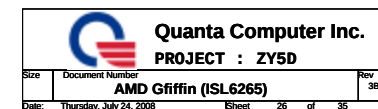


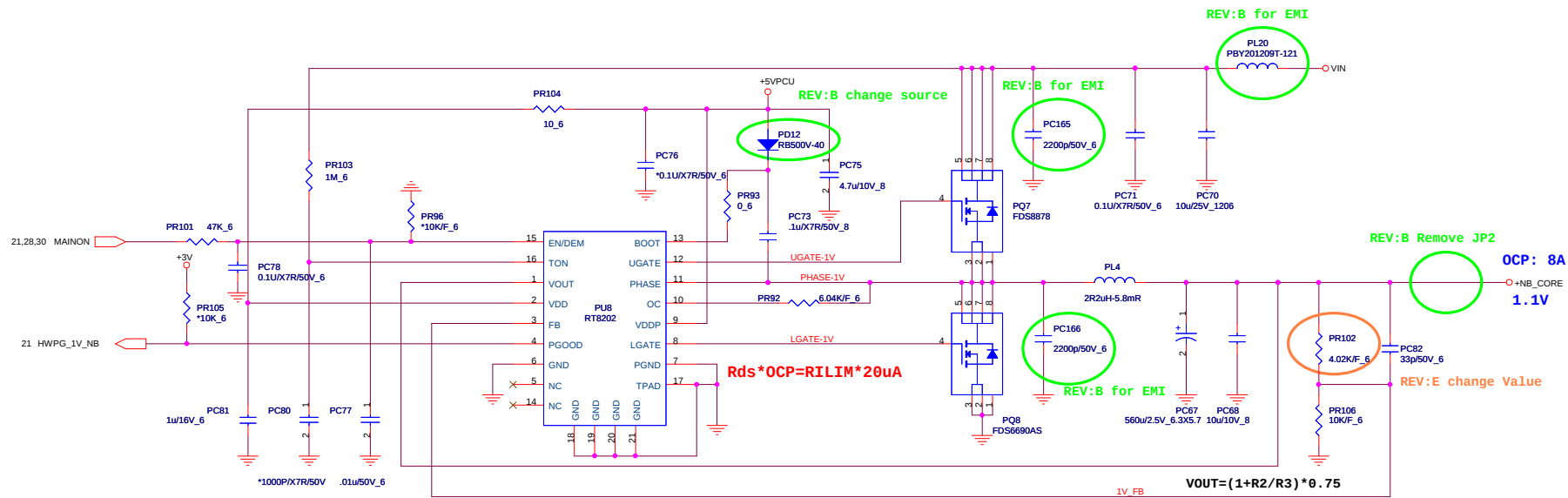
Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	PCMCIA(OZ601)	3B
Date:	Wednesday, May 21, 2008	Sheet 23 of 35



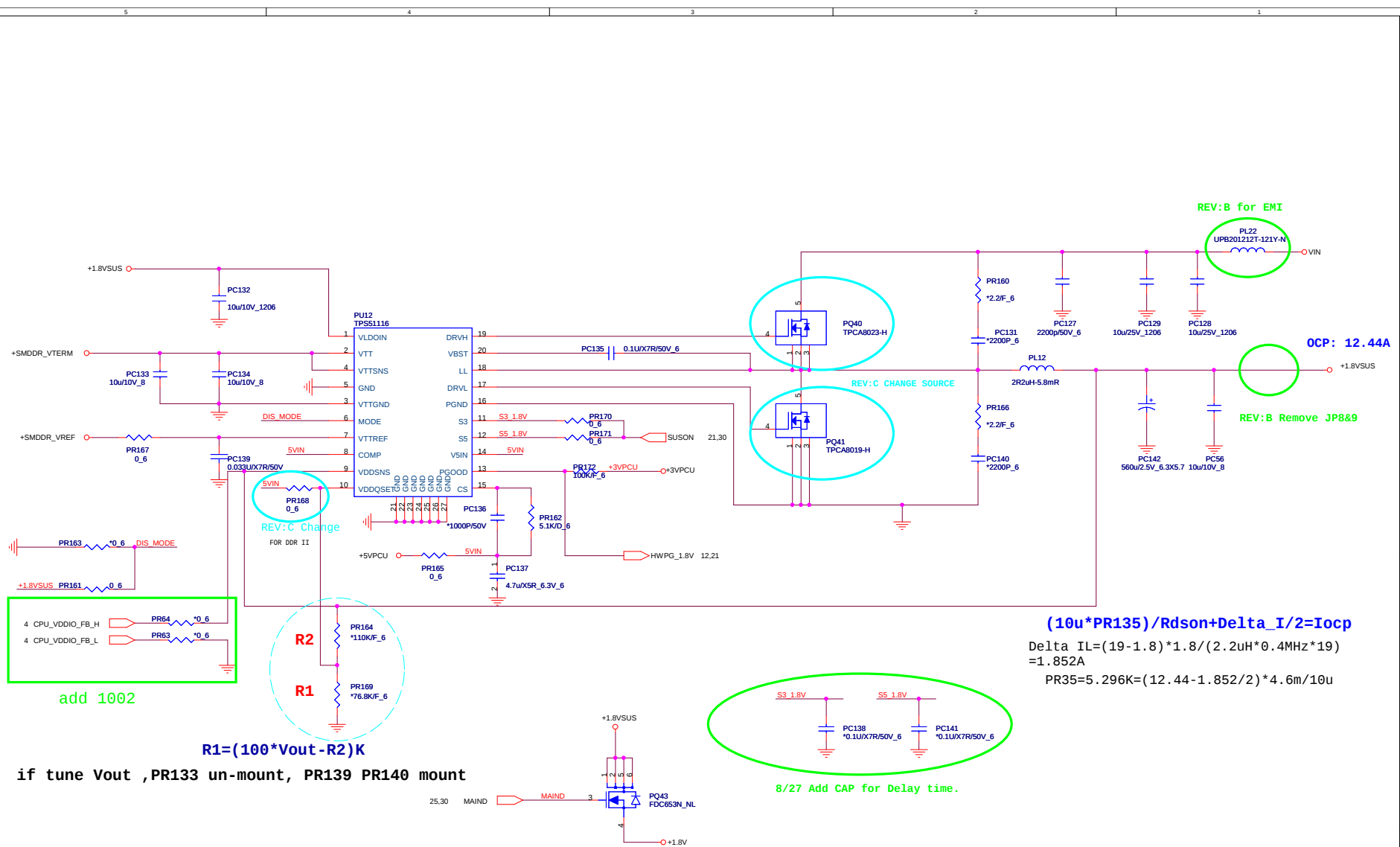
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)

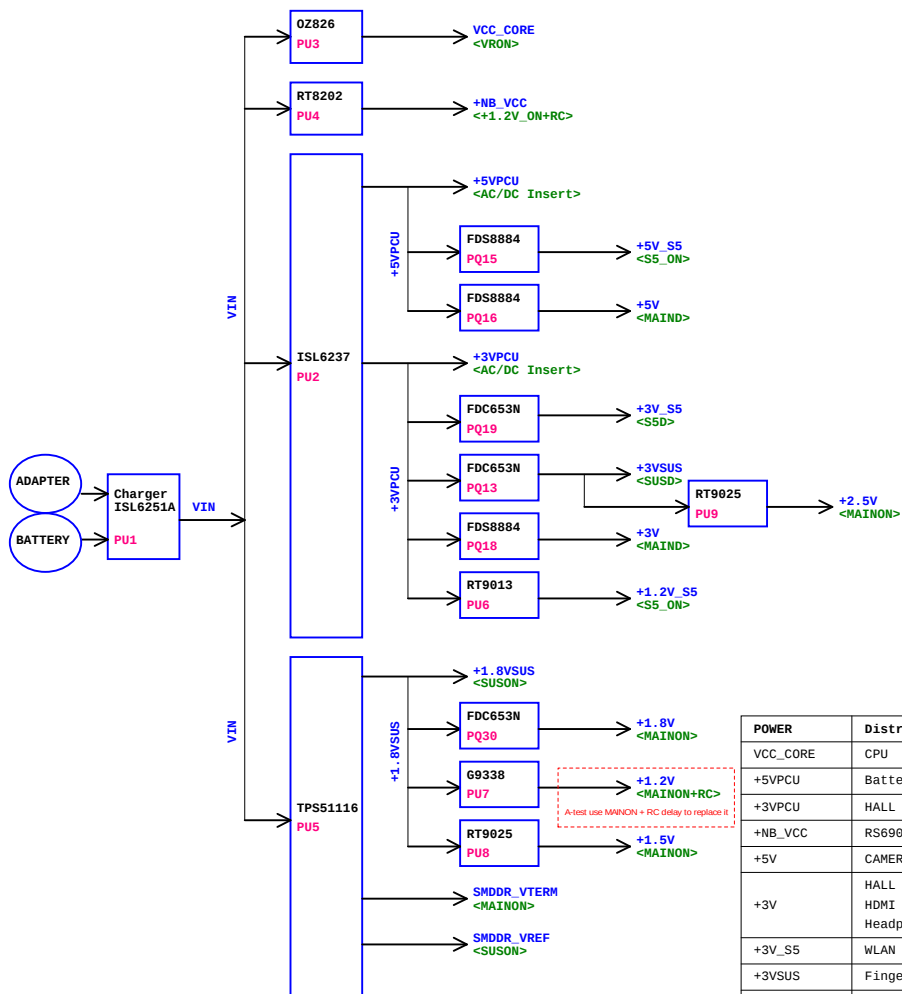
8A OCP --- OC=6.04K
FDS6690AS Rds=15mOhm



$$(10u \cdot PR135) / R_{dson} + \Delta I / 2 = I_{ocp}$$

$$\Delta I_L = (19 - 1.8) \cdot 1.8 / (2.2uH \cdot 0.4MHz \cdot 19) = 1.852A$$

$$PR35 = 5.296K = (12.44 - 1.852 / 2) \cdot 4.6m / 10u$$



POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_VCC	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

ZY5 Power on Sequence

